AF/2811
#13/EOF

PTO/SB/17 (01-03)
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FEE TRANSMITTAL for FY 2003

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 430.00

Complete if Known	
Application Number	09/660,186-Conf. #6720
Filing Date	September 12, 2000
First Named Inventor	Dong-Yeung Kwak
Examiner Name	S. Loke
Group Art Unit	2811
Attorney Docket No.	8733.298.00US

METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit Card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account

Deposit Account Number: 50-0911

Deposit Account Name: McKenna Long & Aldridge LLP

The Commissioner is hereby authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee**

to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		x		=	
Independent Claims		-3** =		x		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	110.00
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	320.00
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify)					

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 430.00

SUBMITTED BY				Complete *(if applicable)*	
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DC:118811.1

#14/Appeal Brief OKON

Docket No.: 8733.298.00-US
(PATENT)

3/3/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Dong Yeung KWAK

Application No.: 09/660,186 Group Art Unit: 2811

Filed: September 12, 2000 Examiner: S. LOKE

For: TFT LCD

APPELLANTS'S BRIEF

Attention: Board of Patent Appeals and Interferences
Commissioner for Patents
Washington, DC 20231

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on December 16, 2002.

The fees required under § 1.17(f) and any required petition for extension of time for filing this brief and fees therefore are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. Real Party In Interest

II Related Appeals and Interferences

III. Status of Claims

REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Dong Yeung Kwak and LG.Philips LCD Co., Ltd.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Total Number of Claims in Application

There are 18 claims pending in application.

Current Status of Claims

Claims canceled: 1 and 8.

Claims withdrawn from consideration but not canceled: N/A

Claims pending: 2-7 and 9-20

Claims allowed: N/A

Claims rejected: 2-7 and 9-20

Claims On Appeal

The claims on appeal are claims 2-7 and 9-20.

STATUS OF AMENDMENTS

The Examiner issued a Final Rejection on August 9, 2002. Appellants filed a Request for Reconsideration on November 6, 2002. The claims were not amended after the final rejection. The Examiner responded to the Request for Reconsideration in an Advisory Action mailed November 19, 2002. In the Advisory Action, the Examiner indicated that Applicants' remarks in the Request for Reconsideration were considered, but did not place the application in condition for allowance. Appellants filed a Notice of Appeal on December 16, 2002.

Accordingly, the claims enclosed herein as Appendix A reflect the originally filed claims 14 and 16-20, and amended claims 2-7, 9-13, and 15.

SUMMARY OF INVENTION

The present invention relates to a thin film transistor liquid crystal display (TFT LCD) having a large aperture ratio.

An object of the present invention is to provide a TFT LCD in which an effective voltage to liquid crystal is stabilized, for making a stable operation.

Another object of the present invention is to provide a TFT LCD which can maintain a fixed capacitance between a scanning line and a drain electrode even if the scanning line and the signal line are misaligned.

Another object of the present invention is to provide a TFT LCD which shows no deterioration of a picture quality even in divided exposure for a large sized screen.

A further object of the present invention is to provide a TFT LCD which has an improved aperture ratio.

ISSUES

The first issue is whether the Examiner properly rejected claims 2 and 4-7 under 35 U.S.C. § 102(e) as being anticipated by Ono et al. (US Patent No. 6,377,323).

The second issue is whether the Examiner properly rejected claims 3 and 9-20 under 35 U.S.C. § 103(a) as being unpatentable over Ono et al. (US Patent No. 6,377,323).

GROUPING OF CLAIMS

For purposes of this appeal brief only, and without conceding the teachings of any prior art reference, the claims have been grouped as indicated below:

Group/Claim(s)

A. Independent claim 2 and its dependent claims 3, 4-7;

B. Dependent claim 3, independent claim 9 and its dependent claims 10-14, and independent claim 15 and its dependent claims 16-20.

In Section VIII below, Appellants have included arguments supporting the separate patentability of each claim group as required by M.P.E.P. § 1206.

ARGUMENTS

The Examiner improperly rejected claims 2 and 4-7 under 35 U.S.C. § 102(e) Ono et al. (US Patent No. 6,377,323).

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Note that, in some circumstances, it is permissible to use multiple references in a **35 U.S.C. 102** rejection. See **MPEP § 2131.01**.

Claim 2 is allowable at least for the reason that claim 2 recites a combination of elements including a scanning line on the first substrate; a signal line formed to cross the scanning line, wherein the signal line does not include an extension pattern; a channel layer formed along the signal line and extended to a portion of the scanning line; source and drain electrodes formed separated on the channel layer over the scanning line; a pixel electrode connected to the drain electrode; wherein the drain electrode is parallel to the signal line.

In the Final Office Action, the Examiner refers to the element [GL] as the scanning line and the element [DL] as being both the signal line and the drain electrode. On page 3 of the Final Office Action, the Examiner states that Ono et al. discloses a drain electrode [DL] that is parallel to the signal line [DL], and on page 3, that it is inherent that the pixel electrode is connected to the drain electrode. However, Appellants submit that the cited reference does not teach source and drain electrodes formed separated on the channel layer over the scanning line; a pixel electrode connected to the drain electrode; wherein the drain electrode is parallel to the signal line as recited by claim 2.

The drain electrode 117b of the present invention is extended toward and overlaps the scanning line 111 instead of the signal line. The drain electrode 117b of the present invention is connected to the pixel electrode 121. Appellants submit that the drain electrode in the cited reference is not over the scanning line, parallel to the signal line, and connected to the pixel electrode.

In the cited reference, the drain electrode [DL] referred to by the Examiner overlaps the gate line [GL], and a gate electrode of the TFT is formed in a protruding portion of the scanning line. Column 4, lines 7-25 of Ono et al. The data line constitutes the drain electrode in column 4, lines 26-49. A contact hole CN is provided for connecting the source electrode SD1 to the pixel electrode ITO1 as described in column 7, lines 41-48.

An object of the present invention is to provide a TFT LCD device in which C_{gd}, a parasitic capacitance between the scanning line and a drain electrode, has a constant value by overlapping a pattern extended from the drain electrode with the scanning line completely. Specification at page 7. This constant value is possible although misalignment may occur during processing steps, thereby overcoming problems generated by variation of C_{gd}. Specification at page 6.

In contrast, in Ono et al., the parasitic capacity C_{gs} is a capacity in a region where a pixel electrode is overlapped on the gate line GL with a gate insulator GI and the protective insulating film PSVI interposed therebetween. Column 6, lines 11-17.

The Appellants have achieved advantages according to the present invention by removing an extension of a signal line, forming the drain electrode in parallel with the signal line, and forming the drain electrode and the signal line over the scanning line in the TFT LCD of the present invention.

Appellants submit that each and every feature of independent claim 2 is not present in the cited reference either expressly or inherently described. Moreover, claims

4-7 stand or fall together with claim 2, as they are dependent therefrom, and are believed to be allowable by virtue of their dependence on claim 2, which is believed to be allowable. Appellants request that the rejection under 35 USC § 102(e) be withdrawn. The Examiner improperly rejected claims 3 and 9-20 under 35 U.S.C. § 103(a) as being unpatentable over Ono et al. (US Patent No. 6,377,323).

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.
>
> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claim 9 is allowable at least for the reason that claim 9 recites a combination of elements including a plurality of scanning lines on the first substrate; a channel layer on the gate insulating layer to cross the scanning lines having a portion extended to a top of at least one of the plurality of scanning lines; source and drain electrodes formed separated on the channel layer over the scanning lines; a signal line formed as a unit with the source electrode along the channel layer which is formed to cross the scanning lines, wherein the signal line does not include an extension pattern; a pixel electrode connected to the drain electrode on the protection film; wherein the drain electrode is parallel to the signal line.

Claim 15 is allowable at least for the reason that claim 15 recites a combination of elements including a scanning line on the first substrate; a signal line formed to cross the

scanning line to cover a portion of the channel layer, wherein the signal line does not include an extension pattern; a drain electrode formed on the channel layer spaced a distance away from the signal line in parallel to the signal line; a pixel electrode formed on the protection film connected to the drain electrode; wherein the drain electrode is parallel to the signal line.

As discussed above, Ono et al. does not teach all of the features of the present invention, including features describing the relationship of the drain electrode with other elements. Further, the cited reference does not teach a channel layer on the gate insulating layer to cross the scanning lines having a portion extended to a top of at least one of the plurality of scanning lines as recited by claim 9. The cited reference does not teach a drain electrode formed on the channel layer spaced a distance away from the signal line in parallel to the signal line as recited by claim 15.

However, Ono et al. does not teach or suggest the claimed invention as a whole. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983); see also *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976). The invention of this application includes a thin film transistor liquid crystal display that maintains a constant capacitance between the scanning line and the drain electrode by overlapping a pattern extended from the drain electrode with the scanning line completely. Ono et al. may teach features of a TFT that impact a parasitic capacity, but the reference fails to teach or suggest explicitly or implicitly providing a thin film transistor using the specific features as recited by claims 3, and 9-20.

Applicant has discovered the source of a problem and through experimentation, has identified a solution. Ono et al. is not attempting to solve similar problems related to device degradation with the same solution. "[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole', which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103." *In re Sponnoble*, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). However, "discovery of the cause of a problem . . . does not always result in a patentable invention. . . . [A] different situation exists where the solution is obvious from prior art which contains the same solution for a similar problem." *In re Wiseman*, 596 F.2d 1019, 1022, 201 USPQ 658, 661 (CCPA 1979) (emphasis in original).

Appellants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness with regards to claims 9 and 15 and therefore, the rejection should be withdrawn.

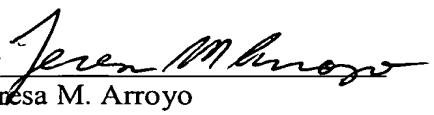
Claims 10-14 and 16-20 stand or fall together with claims 9 and 15, as they are dependent from independent claims 9 and 15, respectively. Claims 10-14 and 16-20 are also allowable by virtue of their dependence on claims 9 and 15, which are believed to be allowable.

CLAIMS INVOLVED IN THE APPEAL

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

Dated: February 24, 2003

Respectfully submitted,

By 

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/660,186

2. A TFT LCD (thin film transistor liquid crystal display) comprising:

a first substrate and a second substrate;

a scanning line on the first substrate;

a signal line formed to cross the scanning line, wherein the signal line does not include an extension pattern;

a channel layer formed along the signal line and extended to a portion of the scanning line;

source and drain electrodes formed separated on the channel layer over the scanning line;

a pixel electrode connected to the drain electrode; and

a liquid crystal layer formed between the first substrate and the second substrate;

wherein the drain electrode is parallel to the signal line.

3. A TFT LCD as claimed in claim 2, wherein the channel layer has a width smaller than a width of the signal line and the scanning line.

4. A TFT LCD as claimed in claim 2, further comprising a gate insulating layer between the scanning line and the channel layer.

5. A TFT LCD as claimed in claim 2, further comprising an ohmic contact layer between the source and drain electrodes and the channel layer.

6. A TFT LCD as claimed in claim 2, wherein the source electrode and the signal line are formed as a unit.

7. A TFT LCD as claimed in claim 2, wherein the drain electrode is overlapped with the scanning line.

9. (Amended) A TFT LCD comprising:

a first substrate and a second substrate;

a plurality of scanning lines on the first substrate;

a gate insulating layer on an entire surface inclusive of the scanning lines;

a channel layer on the gate insulating layer to cross the scanning lines having a portion extended to a top of at least one of the plurality of scanning lines;

source and drain electrodes formed separated on the channel layer over the scanning lines;

a signal line formed as a unit with the source electrode along the channel layer which is formed to cross the scanning lines, wherein the signal line does not include an extension pattern;

a protection film formed on an entire surface inclusive of the signal line;

a pixel electrode connected to the drain electrode on the protection film; and,

a liquid crystal layer formed between the first substrate and the second substrate;

wherein the drain electrode is parallel to the signal line.

10. A TFT LCD as claimed in claim 9, wherein the drain electrode crosses the scanning line.

11. A TFT LCD as claimed in claim 9, wherein the channel layer has a width smaller than a width of the signal line and the scanning line.

12. A TFT LCD as claimed in claim 9, further comprising an ohmic contact layer between the source and drain electrodes and the channel layer.

13. A TFT LCD as claimed in claim 9, wherein the scanning line has a portion enlarged in the vicinity of the signal line.

14. A TFT LCD as claimed in claim 13, wherein the channel layer is formed along the signal line over the scanning line, and has a width enlarged as much as a width of the scanning line is enlarged.

15. (Amended) A TFT LCD having a first substrate, a second substrate, and liquid crystal sealed between the first and second substrates, comprising:

a scanning line on the first substrate;

a gate insulating layer on the scanning line;

a channel layer on the gate insulating layer;

a signal line formed to cross the scanning line to cover a portion of the channel layer, wherein the signal line does not include an extension pattern;

a drain electrode formed on the channel layer spaced a distance away from the signal line in parallel to the signal line;

a protection film formed on an entire surface of the first substrate inclusive of the drain electrode; and

a pixel electrode formed on the protection film connected to the drain electrode;

wherein the drain electrode is parallel to the signal line.

16. A TFT LCD as claimed in claim 15, wherein the channel layer is formed along the signal line.

17. A TFT LCD as claimed in claim 16, wherein the channel layer has a width smaller than a width of the signal line and the scanning line.

18. A TFT LCD as claimed in claim 15, wherein the signal line serves as a source electrode disposed opposite to the drain electrode.

19. A TFT LCD as claimed in claim 15, further comprising a gate insulating layer between the scanning line and the channel layer.

20. A TFT LCD as claimed in claim 18, further comprising an ohmic contact layer between the source and drain electrodes and the channel layer.